(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 617 812 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
04.03.1998 Bulletin 1998/10

(21) Application number: **93900172.3**

(22) Date of filing: **14.12.1992**

(51) Int Cl.[6]: **G06F 1/32**

(86) International application number:
PCT/US92/10798

(87) International publication number:
WO 93/12480 (24.06.1993 Gazette 1993/15)

(54) APPARATUS FOR REDUCING COMPUTER SYSTEM POWER CONSUMPTION

VORRICHTUNG ZUR VERMINDERUNG DES ENERGIEVERBRAUCHS EINES RECHNERSYSTEMS

APPAREIL PERMETTANT DE REDUIRE LA CONSOMMATION D'ENERGIE D'UN SYSTEME INFORMATIQUE

(84) Designated Contracting States:
DE FR GB IE SE

(30) Priority: **17.12.1991 US 809301**

(43) Date of publication of application:
05.10.1994 Bulletin 1994/40

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- **IBM TECHNICAL DISCLOSURE BULLETIN vol. 33, no. 4, September 1990, NEW YORK US pages 474 - 477 'TECHNIQUE FOR MONITORING COMPUTER SYSTEM'S ACTIVITY FOR THE PURPOSE OF POWER MANAGEMENT OF A DOS-COMPATIBLE SYSTEM'**
- **PATENT ABSTRACTS OF JAPAN vol. 14, no. 400 (P-1098)29 August 1990 & JP,A,2 151 950 (NEC CORP) 11 June 1990**

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Description

The invention relates to battery powered computer systems, and more particularly, to circuits and methods for reducing the power consumption of the computer system.

Portable computer systems are rapidly developing the capabilities of conventional desktop or floor mounted personal computer systems. Hard disk units are being integrated into portable computers because of the large amounts of information being processed and the large size of many application programs. A floppy disk unit is integrated in the vast majority of portable computers, even if a hard disk unit is installed, to allow loading of information and use of applications requiring key disks, and also to allow use of diagnostic programs. Modems have been integrated into portable computers for some time to allow communications and information transfer between the user and a remote location, for example, the home office. The displays in portable computer systems are becoming much more elaborate and readable. The pixel count on the standard liquid crystal displays (LCD's) utilized is increasing, as is the viewing angle. The use of backlighting allows use of LCD's in low light environments and improves the contrast ratio of the display. More complex circuitry is being installed in portable computers to support these improved peripheral devices and to support the increased speeds and capabilities of the microprocessors utilized in portable computer systems.

The various peripheral devices and high speed circuitry mentioned above consume large amounts of power when operating. This has resulted in problems in portable computer systems because these systems are generally desired to be used in locations where alternating current is not available. This has made it very difficult to provide all the possible functionality available and yet have an acceptable battery life when the portable computer system is battery powered. Using CMOS components helped reduce the power consumption of the circuitry, but even the use of CMOS components is insufficient at the clock speeds and performance levels of available circuitry. Therefore a dilemma arises whether to provide lesser functionality with longer battery life or greater functionality with lesser battery life or even no battery operation.

Various alternatives were tried to resolve the problem. For example, the International Business Machines (IBM) Corporation PC Convertible included a switch which the user could press to place the computer system in a standby mode. However, the PC convertible was relatively simple, with a low level of functionality as compared to what is currently available, and the requirement of a user action to reduce power consumption limited its use to circumstances where the user remembered to depress the switch. Blanking the display after a period of keyboard inactivity saved power as well as prolonged the life of the display and was widely utilized. A hard disk unit was developed which reduced the power used by the controlling electronics by utilizing only certain portions of the track for servo information and turning off the read channel circuitry until just before a servo burst was expected. Additionally, a programmable value could be provided to the hard disk unit so that after a given inactivity interval defined by this value, the hard disk unit was allowed to spin down and all but some interface circuitry was shut down. While these alternatives did provide some relief, they were not complete solutions to satisfactorily resolve the dilemma, and design tradeoffs still were forced to occur.

U.S. Patent No. 4,980,836 to Carter et al. discloses an apparatus for reducing power consumption in computer systems. The apparatus monitors the address bus to determine when selected peripheral devices have not been accessed for a preset amount of time. When the preset amount of time has passed, the system powers itself down and disables the system clock, placing the system in a standby mode. The system clock could be stopped in this invention because the preferred embodiment of this invention used a static CMOS processor and chip set. If there was sufficient energy in the batteries, the system could be awakened by the user depressing a standby switch. Computer systems which do not use a static CMOS processor or chip set generally reduce the clock frequency when a preset amount of time of address bus inactivity has passed. Reducing the clock frequency during inactive periods reduces power consumption during this time. However, the frequency of peripheral device accesses is not a completely reliable indicator of inactivity of a computer system. Thus, in some instances the system clocking signal may be reduced in frequency or disabled during a period of high computer system activity. Therefore, a need arises to monitor other elements or events of the computer system to more reliably determine the activity level of the computer system so that the system clock can properly be adjusted to reduce power consumption.

European Patent Application EP-A-0 451 661 of Matsuzaki et al discloses an apparatus for use with a computer system for reducing power consumption of the computer system, comprising a processor having a clocking input, a memory coupled to the processor, means for producing a clocking signal, the clocking signal having a frequency, a counter coupled to the processor for counting a number of events associated with activity of the processor, means coupled to the counter for periodically reading the counted number of events counted by the counter, means coupled to the periodic reading means and the clocking signal producing means for adjusting the frequency of the clocking signal based on the counted number of events, and means coupled to the adjusting means and the processor for providing the adjusted clocking signal to the processor clocking input.

Such an apparatus is reflected in the preamble of claim 1. The invention additionally comprises the fea-

tures of the characterizing part of claim 1. Advantageous embodiments can be found in the subclaims.

A battery powered computer system according to the present invention determines when the system is not in use by monitoring various events associated with the operation of the computer system. In the preferred embodiment, the system monitors the number of cache read misses and write operations, i.e., the cache hit rate, and reduces the system clock frequency when the cache hit rate rises above a certain level. When the cache read hit rate is above a certain level, then it can be assumed that the processor is executing a tight loop, such as when the processor is waiting for a key to be pressed. In an alternate embodiment of the invention, the system monitors other events in addition to the cache read hit rate, such as the occurrence of page hits or input/output (I/O) write cycles, to determine the level of activity of the computer system.

The system according to the preferred embodiment includes a frequency switching circuit, an event counter, and a periodic timer. The event counter is preferably used to measure the incidence of cache read misses and write operations and may also optionally be used to count the number of page misses and memory or I/O writes as desired. The event counter includes an overflow or carry line which prevents any further incrementing of the counter once the maximum number of counts is reached to prevent the counter from overflowing. The periodic timer instructs the CPU via a system interrupt to periodically monitor and compare the contents of the event counter. Every event increments the counter and, the more events, the more processor activity that is presumed. When the periodic timer issues a system interrupt, the CPU reads the contents of the counter and compares the event activity with a predetermined value. If the number of events is higher than the predetermined value, then the processor switches the operating frequency of the system to a high frequency if the system is not already operating at this high frequency. A lower event count causes the frequency switching circuit to switch to a lower frequency to conserve power if the system is not already operating at this low frequency.

The invention allows the battery powered operating period of a computer system to be greatly extended without requiring any input from the user and without any noticeable loss in processing power. This allows a battery powered computer system to have advanced capabilities and functionality while still having a satisfactory battery operating interval.

A better understanding of the invention can be obtained when the following detailed description of the preferred embodiment is considered in conjunction with the following drawing in which:

Figure 1 is a schematic block diagram of a computer system incorporating the present invention;
Figure 2 is a more detailed schematic diagram of a portion of the computer system of Figure 1;
Figure 3 is a schematic diagram of a portion of the computer system of Figure 1 according to an alternate embodiment of the invention; and
Figure 4 is a flowchart diagram of a sequence for controlling the operation of the computer system of Fig. 1 according to the present invention.

Referring now to Figure 1, a computer system C according to the preferred embodiment of the invention is shown. The computer system C is preferably based on the 386 SL chip set produced by Intel Corporation (Intel). The 386 SL chip set comprises two chips, a 386 SL CPU chip (CPU chip) 20 and a 82360 SL chip 22. The CPU chip 20 includes an 80386 SX microprocessor, a memory controller, a cache controller, a bus controller, clock control circuitry, and power management circuitry. The 82360 SL chip 22 includes a programmable interrupt controller (PIC), direct memory access (DMA) controller, a memory mapper, various ports, a real time clock (RTC) and power management circuitry. For more information on the 386 SL chip set, please see the Intel 386 SL Microprocessor Superset System Design Guide 1990 edition; the 386 SL Microprocessor Superset Programmers Reference Manual, 1990 edition; and the 386 SL Microprocessor Superset Data Book; all published by Intel.

An oscillator 24 is connected to the CPU chip 20. The oscillator preferably operates at 20 Megahertz (MHz) and provides a 20 MHz clocking signal 25 to the CPU chip 20. Main memory 26, cache memory 28 and a math coprocessor (MCP) 30 are also preferably coupled to the CPU chip 20. The math coprocessor 30 is preferably a 387 SX coprocessor produced by Intel. The cache memory is preferably operated as a write-through cache memory. A video graphics array (VGA) controller 32 is coupled to the CPU chip 20. Serial port buffers 36 and a parallel port 38 are coupled to the 82360 SL chip 22.

The CPU chip 20 and the 82360 SL chip 22 are each connected to an I/O bus 40 based on the industry standard architecture (ISA). However, other bus architectures are also contemplated. The ISA bus 40 is connected through a transceiver 42 to a peripheral interface (PI) bus 44. The VGA chip 32 is connected to the ISA bus 40. The ISA bus 40 may include a plurality of ISA bus expansion slots 46 if the present invention is used in a desktop computer system. The slots 46 are generally omitted in portable computers. The ISA bus 40 is connected through a transceiver 48 to a hard disk 50. Various logic is coupled to the PI bus 44, including an external real time clock 54, a floppy disk controller 56, a keyboard controller 58 and BIOS EPROM 60. The floppy disk controller 56 and keyboard controller 58 control operation of a floppy disk unit and keyboard, respectively (both not shown). The BIOS EPROM holds the basis input/output (I/O) system software as well as system-specific initialization and configuration software. This is an exemplary computer system and other designs and architectures could be utilized.

The CPU chip 20 includes an active high input referred to as the TURBO input (not shown). When the TURBO input receives a logic high signal, the CPU chip 20 enters "turbo mode," and the microprocessor executes at a clock speed defined by a bit field in a register in the CPU chip 20 referred to as the CPUWRMODE register (not shown). When the TURBO input receives a logic low signal, the CPU chip 20 enters "de-turbo mode" and executes at a reduced clock speed of ½ or ¼ as defined by a bit in a register. The CPUWRMODE register operates in conjunction with the power management circuitry inside the CPU chip 20 to control the frequency of the clocking signal 25 provided to the microprocessor. In the preferred embodiment, the turbo input receives a logic high value, and thus the CPUWRMODE register determines the frequency of the clocking signal 25 provided to the microprocessor.

Bits 5 and 4 of the CPUWRMODE register determine the speed with which the microprocessor clock operates. When bits 5 and 4 of the CPUWRMODE register are each set to 0, then the clock speed is the speed of the signal received by the oscillator 24, preferably 20 MHz. When bits 5 and 4 of the CPUWRMODE register are set to 0 and 1 respectively, the clock speed provided to the microprocessor is one half of the frequency of the signal received from the oscillator 24, i.e., 10 MHz. When bits 5 and 4 of the CPUWRMODE register are 1 and 0 respectively, the clock speed provided to the microprocessor is one fourth of the frequency of the signal received from the oscillator 24, i.e., 5 MHz. When bits 5 and 4 of the CPUWRMODE register each have a logic 1 value, then the clock speed provided to the CPU is one eighth the frequency of the signal received from the oscillator 24, i.e. 2.5 MHz.

The computer system C also includes activity monitor logic 70 according to the present invention which is coupled to the CPU chip 20. The activity monitor logic 70 receives signals from the CPU chip 20 as well as signals provided from the CPU chip 20 to the main memory 26. The activity monitor logic 70 monitors events associated with the microprocessor to determine the activity level of the system. In the preferred embodiment, the activity monitor logic 70 monitors the number of cache read misses and write operations during preset periods of time, and the CPU chip 20 reduces the system clock frequency when the cache hit rate rises above a certain level. When the cache read hit rate is above a certain level, then it can be assumed that the processor is executing a tight loop, such as when the processor is waiting for a key to be pressed. In this instance, the system clock frequency can be reduced to reduce power consumption without affecting system performance. In an alternate embodiment of the invention, the activity monitor logic 70 monitors other events such as page misses or memory and I/O write operations, among others. It is contemplated that the various types of events may be counted either individually or in combination.

Referring now to Figure 2, the activity monitor logic 70 according to the preferred embodiment of the invention is shown. In the description that follows a signal name followed by an asterisk indicates that the signal is asserted when it has a logic low level. The activity monitor logic 70 receives column address strobe (CAS*) signals provided from the CPU chip 20 to the main memory 26. The CAS* signals are essentially memory select signals that are used in paged memory systems. When a cache read hit occurs, the requested data can be provided directly from the cache memory 28 to the microprocessor, and no CAS* signals are asserted by the CPU chip 20. Also, since the cache memory is operated as a write-through cache, each write operation, whether it be a write hit or write miss, requires a memory cycle to the main memory 26. Therefore, the CAS* signals are asserted on all write operations in the preferred embodiment. Thus, the CAS* signals are used to determine when cache read miss operations and write operations occur, i.e., when main memory cycles occur.

In the preferred embodiment, the CPU chip 20 generates eight CAS* signals. The CAS* signals are provided to eight inputs of a nine input NAND gate 102, in effect ORing these signals together. The output of the NAND gate 102 is provided to an input of a two input AND gate 103. A signal referred to as REFREQ output from the 82360 SL chip 22 is preferably provided to the other input of the AND gate 103, which is an inverted input. The REFREQ signal indicates, when asserted high, that a memory refresh operation is occurring. The inverted REFREQ signal is ANDed with the output of the NAND gate 102 to prevent memory refresh operations from being counted as cache read miss or write operations.

The output of the AND gate 103 is a signal referred to as CACHE_MISS, which is provided to the clock input of a 17 bit counter 104 referred to as the CAS* counter. The CACHE_MISS signal is therefore asserted when a main memory cycle occurs, which is whenever a cache read miss or a write operation occurs. The CAS* counter 104 is incremented each time the CACHE_MISS signal is asserted. The CAS* counter 104 outputs a signal referred to as CARRY which is provided through an inverter 106 to the seventh input of the NAND gate 102. The CARRY signal is asserted when the maximum number of counts is reached by the counter 104, which is 2^{17}. When the CARRY signal is asserted, the CACHE_MISS signal is prevented from changing state and thus further counting by the counter 104 is disabled. The CAS* counter 104 provides data signals 1-16 to the inputs of a 16 bit flip-flop 108. Data signal 0 output from the CAS* counter is preferably left unconnected. The outputs of the flip-flop 108 are coupled to data bus signals referred to as DATA<0:15>, which are coupled to the CPU chip 20.

Address signals, a write/read (W/R) signal and a memory/input output (M/IO) signal are output from the CPU chip 20 and provided to decode logic 110 in the activity monitor logic 70. The decode logic 110 outputs

a signal referred to as RD_COUNT which is provided to a clock input of the flip-flop 108. The RD_COUNT signal is also provided through an inverter 111 to an inverted clear input of the counter 104 and to an inverted enable input of the flip-flop 108. Therefore, when the CPU chip 20 desires to read the counter 104, it outputs the appropriate address, the W/R signal and the M/IO signal to the decode logic 110, which then asserts the RD_COUNT signal to the counter 104 and the flip-flop 108. The asserted RD_COUNT signal enables the flip-flop 108 to latch in data from the counter 104 and transmit the data to the CPU chip 20 and simultaneously operates to clear the contents of the counter 104.

In an alternate embodiment, memory page misses and/or I/O write operations may also be counted. Memory page miss operations with the preferred microprocessor are determined by determining if any of the 4 row address strobe or RAS* signals are asserted low during non-refresh cycles. The asserted RAS* signals are indicative of page miss operations. As shown in Figure 3, the RAS* signals are provided from the CPU chip 20 to the inputs of a four input NAND gate 120. The output of the NAND gate 120 is the page miss indication, which is referred to as the PAGE_MISS signal. The I/O write indication is accomplished in the following manner. The W/R signal is connected to an input of a two input AND gate 124. The other input of the AND gate 124 is inverted and receives the M/IO signal. The output of the AND gate 124 generates a signal referred to as IOW which indicates, when asserted high, that an I/O write operation is occurring.

The PAGE_MISS and IOW signals are connected to inputs of a three input OR gate 126. The eight CAS* signals are connected to the input of an eight input NAND gate 125 whose output is connected to an input of the OR gate 126. The output of the OR gate 126 is connected to an input of a three input AND gate 128. A second input of the AND gate 128 receives the inverted CARRY signal. The third inverted input of the AND gate 128 receives the REFREQ signal. The output of the AND gate 128 is provided to the clock input of the counter 104. Therefore, during memory refresh operations or when the CARRY signal is asserted, the output of the AND gate 128 is negated low, and thus the counter 104 does not count at these times.

In this embodiment, cache read miss and write operations, page miss operations, and I/O write operations are all monitored as events. It is noted that any one of these events can be monitored either individually or in combination. In yet another alternate embodiment, each signal can be provided to separate counters arranged like the counter 104, and the outputs of the separate counters can be used to determine system activity.

The 82360 SL chip 22 includes an interrupt timer (not shown) which is used to generate time of day interrupts to the microprocessor approximately 18.2 times per second. The interrupt routine invoked by the timer is also used according to the preferred embodiment of the invention to periodically adjust the frequency of the clocking signal 25 received by the microprocessor, as is explained below.

Referring now to Figure 3, a portion of the software routine that is executed when the time of day interrupt routine is invoked is shown. It is understood that the time of day interrupt routine may perform other operations than those shown. When the time of day interrupt signal is asserted, the CPU chip 20 reads the CAS* counter 104 in step 202. The counter 104 is also cleared in step 202. In an alternative embodiment, the separate counters providing the CAS* count, the memory page miss count, and the I/O write count are read in step 202. In step 204, the microprocessor reads bits 5 and 4 of the CPUWRMODE register to determine if the clock signal provided to the CPU chip 20 is operating at a fast or slow frequency. In the preferred embodiment, the microprocessor only writes either values 0,0 or 1,0 to bits 5 and 4, respectively, of the CPUWRMODE register, thus providing the clocking signal 25 at either full frequency or one quarter frequency to the microprocessor. The CPUWRMODE register is programmed depending on the cache read hit rate as determined by the CAS* counter 104 in relation to certain comparison values. Thus, in this embodiment, the power management logic toggles between a full clock speed or fast speed, preferably 20 MHz, and a one quarter frequency clock speed or slow speed, preferably 5 MHz. However, it is noted that all four clock speed frequencies may be utilized.

If the clocking signal 25 provided to the CPU is determined to be operating at the slow speed in step 204, then in step 206 the microprocessor determines if the CAS* count value received from the CAS* counter 104 is greater than a fast comparison value stored inside the CPU chip 20. Alternatively, a function based on the three separate count values could be evaluated. If the CAS* count value exceeds the fast comparison value in step 206, then in step 208 the power management logic in the CPU chip 20 speeds up the clock signal 25 provided to the microprocessor to the full clock speed, and the routine completes. If the CAS* count value is not greater than the fast comparison value in step 206, then the interrupt routine completes.

If the clocking signal 25 provided to the microprocessor is determined to be operating at the fast speed in step 204, then control proceeds to step 212 where the microprocessor determines whether the CAS* count value is less than a slow comparison value stored in the CPU chip 20. If the CAS* count value is less than the slow comparison value in step 212, then the power management logic in the CPU chip 20 slows down the clocking signal 25 provided to the microprocessor in step 214 to one quarter speed, and the routine completes. If the CAS* count value is not less than the slow comparison value in step 212, then the routine completes.

The fast and slow comparison values are preferably programmable inside the CPU chip 20. In the preferred embodiment, the fast and slow comparison values are

the same value. In an alternate embodiment, the slow comparison value is proportionally less that the fast value, i.e., one fourth less to reflect a true hit/miss ratio. In addition, since the comparison values can be user-adjusted inside the CPU chip 20, the values could be derived from characterization of common user applications.

As described above, the preferred embodiment utilizes the CPU chip 20 in "turbo mode" and uses software to perform the activity comparisons and speed changes. In an alternative embodiment, additional registers can be used to contain the comparison values and an additional timer can be used to define the comparison interval. Hardware comparators are configured to perform the comparison logic described above at the appropriate time and change the state of the TURBO input based on the comparison to speed up or slow down the CPU chip 20 as appropriate.

Thus, the computer system according to the present invention monitors various power consumption related events, indicates certain changes to the user and enters an inactivity state upon an appropriate period of time after monitored system devices have been used.

Claims

1. An apparatus for use with a battery powered computer system (C) for reducing power consumption of the battery powered computer system, comprising:

   a processor (20) having a clocking input;
   memory (6) coupled to the processor;
   means (24) for producing a clocking signal (25), the clocking signal having a frequency;
   a counter (140) coupled to the processor for counting a number of events associated with activity of the processor;
   means (108,110) coupled to the counter for periodically reading the counted number of events counted by the counter;
   means (20) coupled to the periodic reading means and the clocking signal producing means for adjusting the frequency of the clocking signal based on the counted number of events; and
   means (20) coupled to the adjusting means and the processor for providing the adjusted clocking signal to the processor clocking input;

   characterised by;

   cache memory (28) coupled to said processor (20);
   and wherein the events comprise cache read miss operations and memory write operations.

2. The apparatus of claim 1, further comprising:

   means (20) coupled to the adjusting means (20) for determining the current operating frequency of the clocking signal (25); and
   wherein the adjusting means further adjusts the frequency of the clocking signal based on the current operating frequency of the clocking signal.

3. The apparatus of claim 1, wherein the adjusting means (20) includes:

   means for determining if the clocking signal (25) is operating at a higher or a lower frequency;
   means (20) coupled to the periodic reading means (110) for determining if the counted number of events is greater than a first value if the clocking signal is operating at the lower frequency;
   means (20) coupled to the greater than determining means and the clocking signal producing means for increasing the frequency of the clocking signal if the counted number of events is greater than the first value and the clocking signal is operating at the lower frequency;
   means (20) coupled to the periodic reading means for determining if the counted number of events is less than a second value if the clocking signal is operating at the higher frequency; and
   means (20) coupled to the less than determining means and the clocking signal producing means for decreasing the frequency of the clocking signal if the counted number of events is less than the second value and the clocking signal is operating at the higher frequency.

4. The apparatus of claim 3, wherein the first value is equal to the second value.

5. The apparatus of any of claims 1 to 4, further comprising:

   input/output devices coupled to the processor;
   wherein the main memory is organized as paged memory (26);
   wherein the counter further counts the number of input/output write cycles and page miss operations; and,
   wherein the adjusting means adjusts the frequency of the clocking signal additionally based on main memory page miss operations and input/output write operations.

Patentansprüche

1. Vorrichtung zur Verwendung mit einem batteriebetriebenen Computersystem (C) zum Vermindern des Energieverbrauchs des batteriebetriebenen Computersystems, umfassend:

einen Prozessor (20) mit einem Takteingang;

einen mit dem Prozessor verbundenen Speicher (6);

eine Einrichtung (24) zum Erzeugen eines Taktsignals (25), wobei das Taktsignal eine Frequenz aufweist;

einen Zähler (104), der mit dem Prozessor verbunden ist, zum Zählen einer mit der Aktivität des Prozessors verbundenen Anzahl von Ereignissen;

eine Einrichtung (108, 110), die mit dem Zähler verbunden ist, zum periodischen Ablesen der durch den Zähler gezählten Anzahl von Ereignissen;

eine Einrichtung (20), die mit der periodischen Ableseeinrichtung und der Taktsignalerzeugungseinrichtung verbunden ist, zum Justieren der Frequenz des Taktsignals auf der Basis der gezählten Anzahl von Ereignissen und

eine Einrichtung (20), die mit der Justierungseinrichtung und dem Prozessor verbunden ist, zum Anlegen des justierten Taktsignals an den Prozessortakteingang,

gekennzeichnet durch:

einen mit dem Prozessor (20) verbundenen Cachespeicher (28),

und worin die Ereignisse fehlgeschlagene Cache-Leseoperationen und Speicherschreiboperationen umfassen.

2. Vorrichtung nach Anspruch 1, weiter umfassend:

eine Einrichtung (20), die mit der Justierungseinrichtung (20) verbunden ist, zum Bestimmen der augenblicklichen Betriebsfrequenz des Taktsignals (25) und

worin die Justierungseinrichtung des weiteren die Frequenz des Taktsignals auf der Basis der augenblicklichen Betriebsfrequenz des Taktsignals justiert.

3. Vorrichtung nach Anspruch 1, bei der die Justierungseinrichtung (20) umfaßt:

eine Einrichtung zum Bestimmen, ob das Taktsignal (25) bei einer höheren oder einer niedrigeren Frequenz arbeitet;

eine Einrichtung (20), die mit der periodischen Ableseeinrichtung (110) verbunden ist, zum Bestimmen, ob die gezählte Anzahl von Ereignissen größer als ein erster Wert ist, wenn das Taktsignal bei der niedrigeren Frequenz arbeitet;

eine Einrichtung (20), die mit der Größer-als-Bestimmungseinrichtung und der Taktsignalerzeugungseinrichtung verbunden ist, zum Erhöhen der Frequenz des Taktsignals, wenn die gezählte Anzahl von Ereignissen größer als der erste Wert ist und das Taktsignal bei der niedrigeren Frequenz arbeitet;

eine Einrichtung (20), die mit der periodischen Ableseeinrichtung verbunden ist, zum bestimmen, ob die gezählte Anzahl von Ereignissen kleiner als ein zweiter Wert ist, wenn das Taktsignal bei der höheren Frequenz arbeitet, und

eine Einrichtung (20), die mit der Kleiner-als-Bestimmungseinrichtung und der Taktsignalerzeugungseinrichtung verbunden ist, zum Vermindern der Frequenz des Taktsignals, wenn die gezählte Anzahl von Ereignissen kleiner als der zweite Wert ist und das Taktsignal bei der höheren Frequenz arbeitet.

4. Vorrichtung nach Anspruch 3, bei der der erste Werte gleich dem zweiten Wert ist.

5. Vorrichtung nach einem der Ansprüche 1 bis 4, weiter umfassend:

mit dem Prozessor verbundene Eingabe/Ausgabe-Einrichtungen,

worin der Hauptspeicher als Seitenspeicher (26) organisiert ist;

worin der Zähler des weiteren die Anzahl von Eingabe/Ausgabe-Schreibzyklen und fehlgeschlagenen Seitenoperationen zählt und

worin die Justierungseinrichtung die Frequenz des Taktsignals zusätzlich auf der Basis fehlgeschlagener Hauptspeicherseitenoperationen und Eingabe/Ausgabe-Schreiboperationen justiert.

Revendications

1. Un dispositif prévu pour l'utilisation avec un système informatique (C) alimenté par batterie, pour réduire la consommation d'énergie du système informatique alimenté par batterie, comprenant :

   un processeur (20) ayant une entrée d'horloge;
   une mémoire (6) connectée au processeur;
   des moyens (24) pour produire un signal d'horloge (25), le signal d'horloge ayant une fréquence;
   un compteur (140) connecté au processeur pour compter un nombre d'événements associés à l'activité du processeur;
   des moyens (108, 110) connectés au compteur pour lire périodiquement le nombre d'événements qui est compté par le compteur;
   des moyens (20) connectés aux moyens de lecture périodique et aux moyens de génération de signal d'horloge, pour régler la fréquence du signal d'horloge sur la base du nombre d'événements qui est compté; et
   des moyens (20) connectés aux moyens de réglage et au processeur pour appliquer à l'entrée d'horloge du processeur le signal d'horloge réglé;

   caractérisé par :

   une antémémoire (28) connectée au processeur (20);
   et par le fait que les événements comprennent des opérations d'échec de lecture d'antémémoire et des opérations d'écriture en mémoire.

2. Le dispositif de la revendication 1, comprenant en outre :

   des moyens (20) connectés aux moyens de réglage (20) pour déterminer la fréquence de fonctionnement courante du signal d'horloge (25); et
   dans lequel les moyens de réglage règlent en outre la fréquence du signal d'horloge sur la base de la fréquence de fonctionnement courante du signal d'horloge.

3. Le dispositif de la revendication 1, dans lequel les moyens de réglage (20) comprennent :

   des moyens pour déterminer si le signal d'horloge (25) fonctionne à une fréquence supérieure ou une fréquence inférieure;
   des moyens (20) connectés aux moyens de lecture périodique (110) pour déterminer si le nombre d'événements qui est compté est supérieur à une première valeur, si le signal d'horloge fonctionne à la fréquence inférieure;
   des moyens (20) connectés aux moyens de détermination de supériorité et aux moyens de génération de signal d'horloge, pour augmenter la fréquence du signal d'horloge si le nombre d'événements qui est compté est supérieur à la première valeur et le signal d'horloge fonctionne à la fréquence inférieure;
   des moyens (20) connectés aux moyens de lecture périodique pour déterminer si le nombre d'événements qui est compté est inférieur à la seconde valeur, si le signal d'horloge fonctionne à la fréquence supérieure; et
   des moyens (20) connectés aux moyens de détermination d'infériorité et aux moyens de génération de signal d'horloge, pour diminuer la fréquence du signal d'horloge si le nombre d'événements qui est compté est inférieur à la seconde valeur et le signal d'horloge fonctionne à la fréquence supérieure.

4. Le dispositif de la revendication 3 dans lequel la première valeur est égale à la seconde valeur.

5. Le dispositif de l'une quelconque des revendications 1 à 4, comprenant en outre :

   des dispositifs d'entrée/sortie connectés au processeur;
   dans lequel la mémoire centrale est organisée en mémoire paginée (26);
   dans lequel le compteur compte en outre le nombre de cycles d'écriture d'entrée/sortie et d'opérations d'échec de page; et
   dans lequel les moyens de réglage règlent la fréquence du signal d'horloge en se basant en outre sur des opérations d'échec de page de mémoire centrale et des opérations d'écriture d'entrée/sortie.

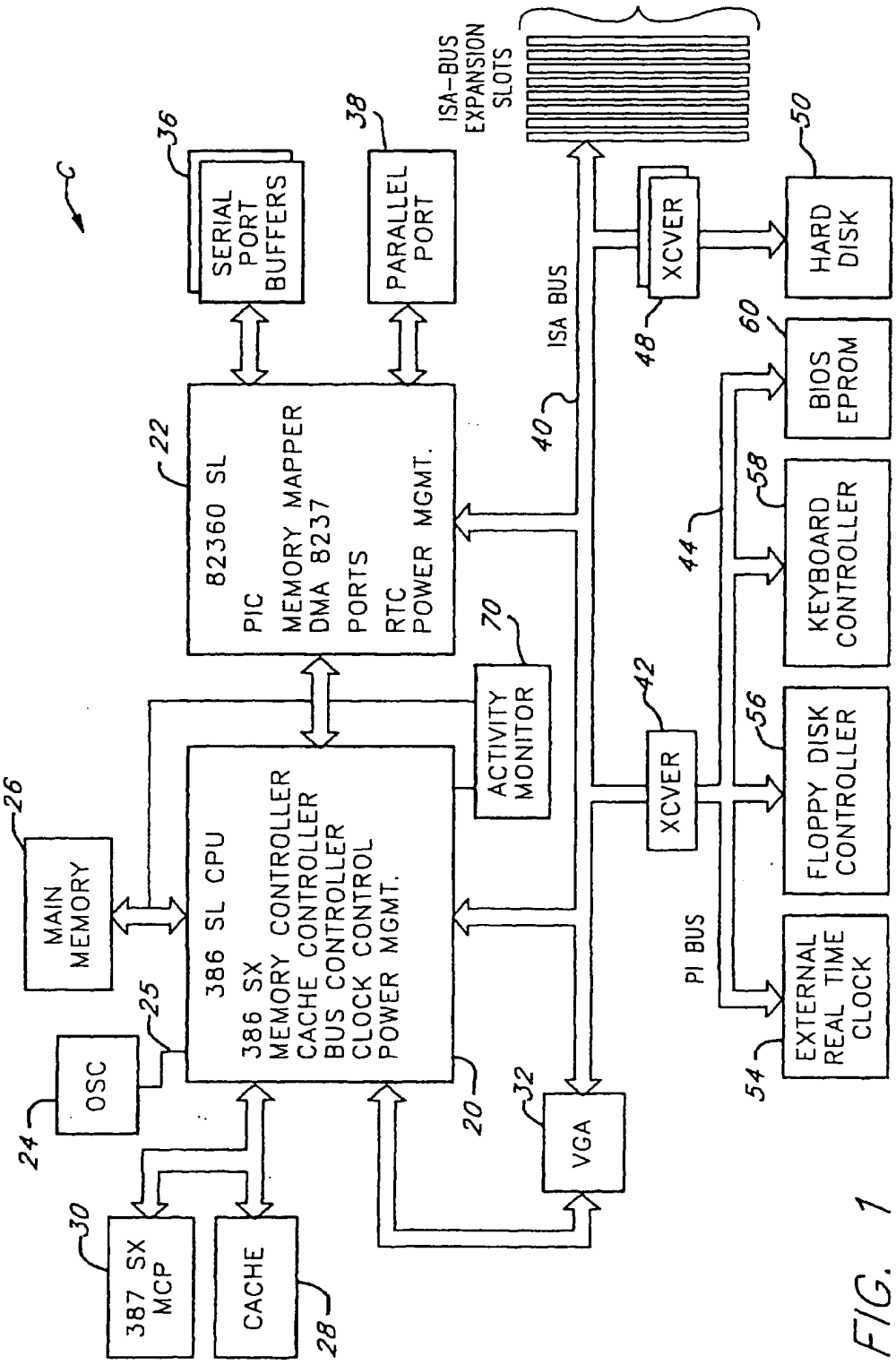
C
SERIAL PORT BUFFERS
36
PARALLEL PORT
38
ISA-BUS EXPANSION SLOTS
82360 SL
PIC
MEMORY MAPPER
DMA 8237
PORTS
RTC
POWER MGMT.
22
ISA BUS
40
XCVER
48
HARD DISK
50
BIOS EPROM
60
KEYBOARD CONTROLLER
58
44
ACTIVITY MONITOR
70
386 SL CPU
386 SX
MEMORY CONTROLLER
CACHE CONTROLLER
BUS CONTROLLER
CLOCK CONTROL
POWER MGMT.
20
XCVER
42
FLOPPY DISK CONTROLLER
56
PI BUS
MAIN MEMORY
26
OSC
24
25
VGA
32
EXTERNAL REAL TIME CLOCK
54
387 SX MCP
30
CACHE
28

FIG. 1

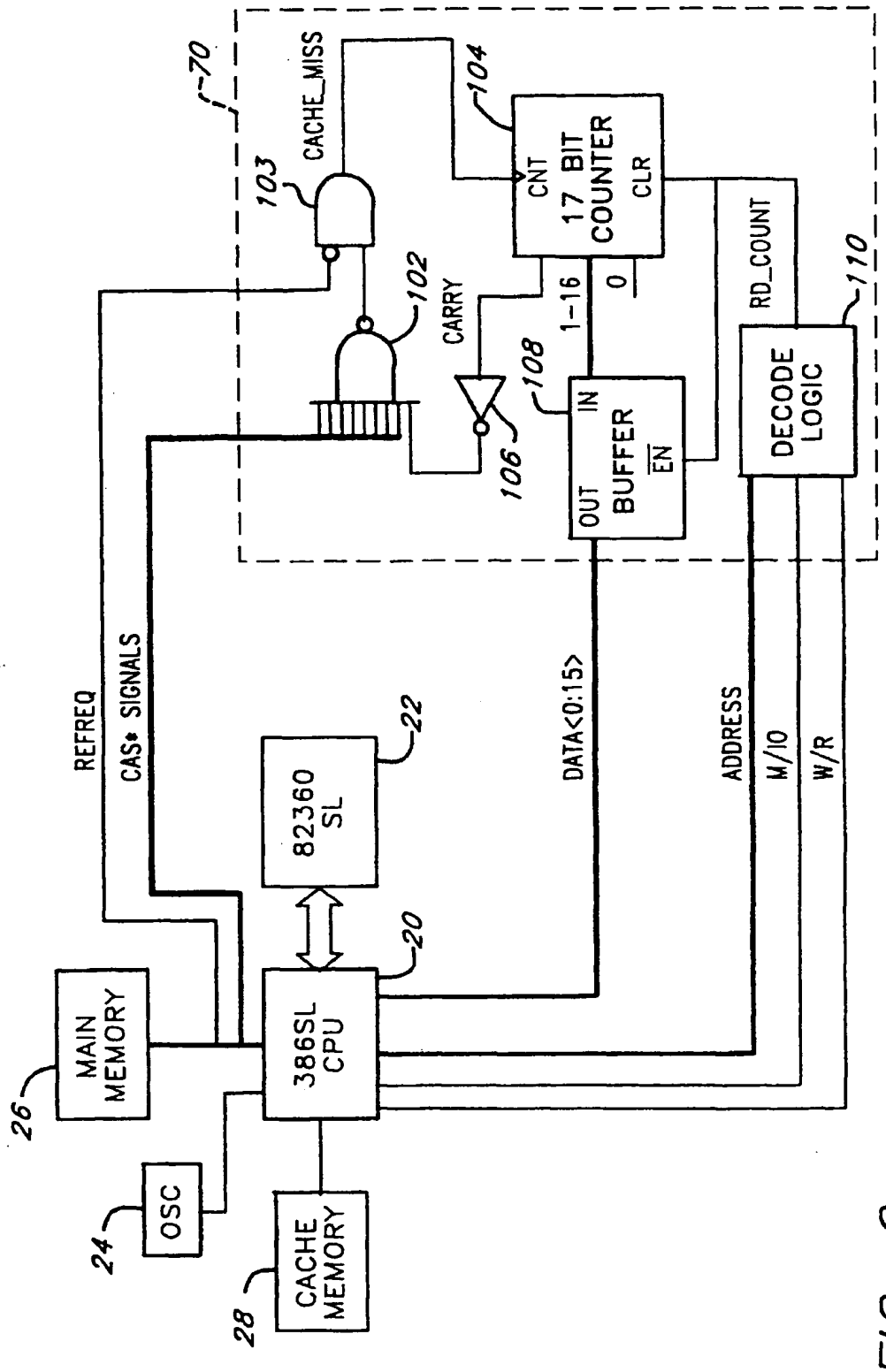
70
CACHE_MISS
103
104
CNT
17 BIT
COUNTER
CLR
102
CARRY
1-16
0
RD_COUNT
110
108
IN
OUT
BUFFER
EN
106
DECODE
LOGIC
REFREQ
CAS* SIGNALS
82360
SL
22
DATA<0:15>
ADDRESS
M/IO
W/R
20
MAIN
MEMORY
386SL
CPU
26
OSC
24
CACHE
MEMORY
28

FIG. 2

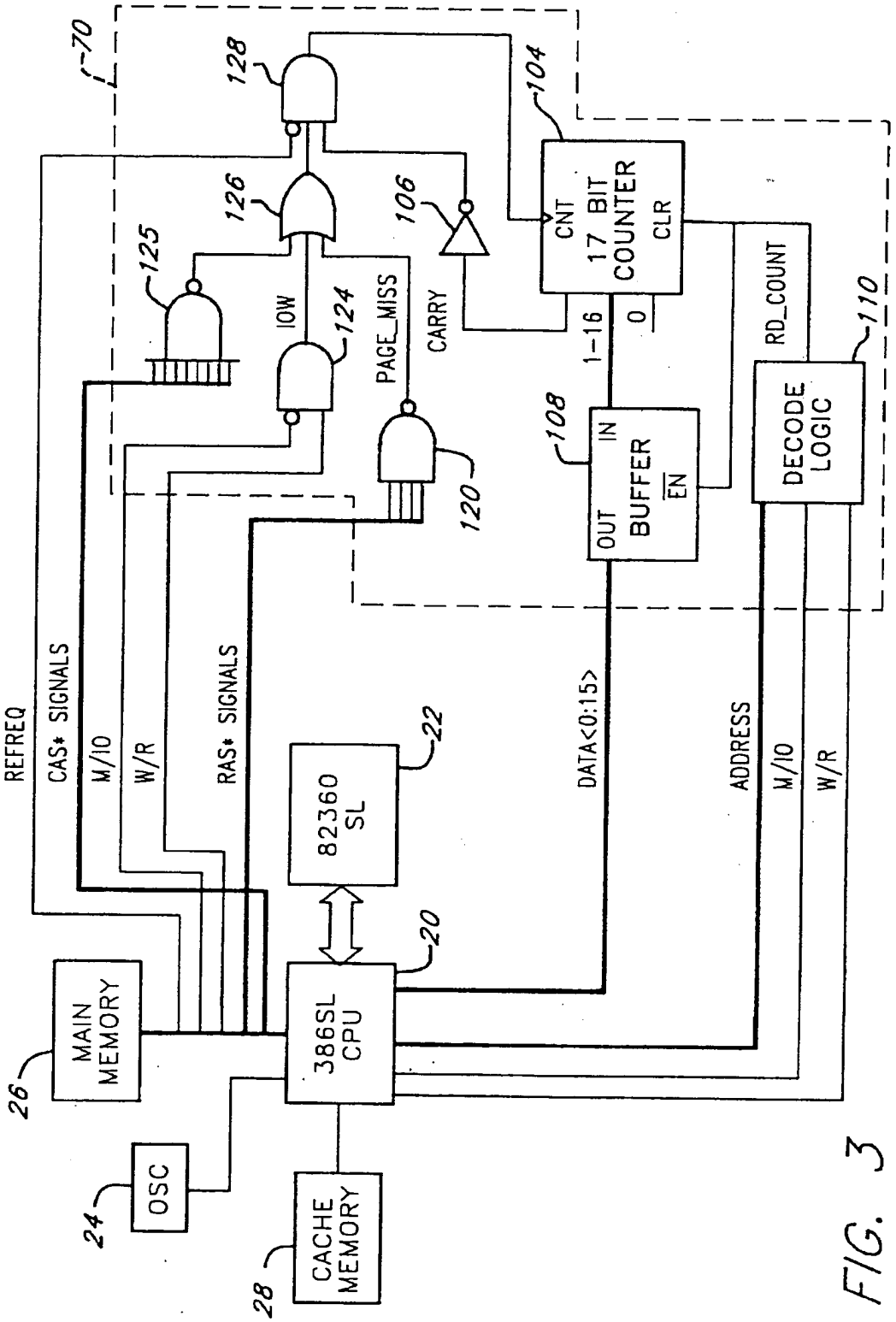
70
128
126
125
124
106
104
CNT
17 BIT
COUNTER
CLR
IOW
PAGE_MISS
CARRY
1-16
0
RD_COUNT
110
108
IN
OUT
BUFFER
EN
DECODE
LOGIC
120
REFREQ
CAS* SIGNALS
M/IO
W/R
RAS* SIGNALS
22
82360
SL
DATA<0:15>
ADDRESS
M/IO
W/R
20
MAIN
MEMORY
26
386SL
CPU
OSC
24
CACHE
MEMORY
28

FIG. 3

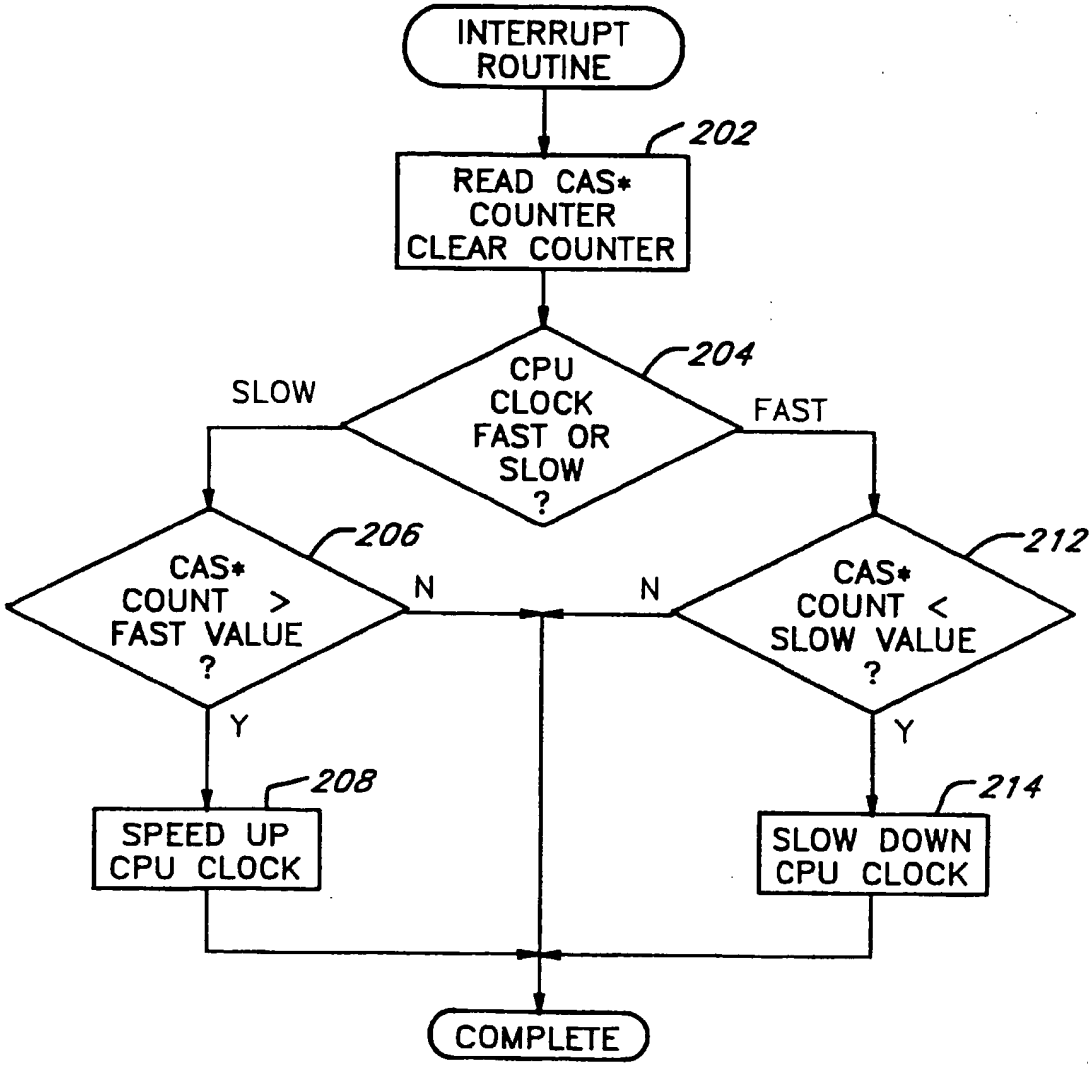
INTERRUPT ROUTINE
202
READ CAS* COUNTER CLEAR COUNTER
204
CPU CLOCK FAST OR SLOW ?
SLOW
FAST
206
CAS* COUNT > FAST VALUE ?
N
N
212
CAS* COUNT < SLOW VALUE ?
Y
Y
208
SPEED UP CPU CLOCK
214
SLOW DOWN CPU CLOCK
COMPLETE

FIG. 4